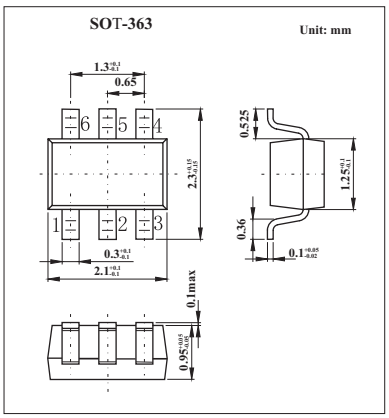
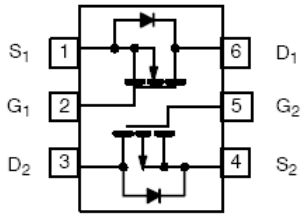
Complementary 20-V (D-S) Low-Threshold MOSFET

KI1501DL



■ PIN Configuration



■ Absolute Maximum Ratings TA = 25℃

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V_{DS}	20	-20	V
Gate-Source Voltage	V_{GS}	±8	±8	V
Continuous Drain Current (T_J = 150℃)* T_A = 25℃	I_D	250	-180	mA
T_A = 70℃		200	-140	mA
Pulsed Drain Current	I_{DM}	500	-500	mA
Maximum Power Dissipation* T_A = 25℃	P_D	0.2		W
T_A = 70℃		0.13		W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		℃
Maximum Junction-to-Ambient*	R_{thJA}	625		℃/W

*Surface Mounted on FR4 Board, t ≤ 10 sec.

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■ Electrical Characteristics T_J = 25℃

Parameter	Symbol	Testconditons		Min	Typ	Max	Unit
Drain Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10μA	N-Ch	20	24		V
		V_{GS} = 0 V, I_D =-10μA	P-Ch	-20	-24		
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 50μA	N-Ch	0.4	0.9	1.5	
		V_{DS} = V_{GS}, I_D = -50 μA	P-Ch	-0.4	-0.9	-1.5	
Gate Body Leakage	I_{GSS}	V_{DS} = 0 V V_{GS} =±8V	N-Ch		±2	±100	nA
			P-Ch		±2	±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	N-Ch		0.001	100	
		V_{DS} = -20 V, V_{GS} = 0 V	P-Ch		-0.001	-100	
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 55℃	N-Ch			1	μA
		V_{DS} = -20 V, V_{GS} = 0 V, T_J = 55℃	P-Ch			-1	
On State Drain Currenta	$I_{D(on)}$	V_{DS} ≥2.5 V, V_{GS} = 5.0 V	N-Ch	120			mA
		V_{DS} ≤-2.5 V, V_{GS} = -5.0 V	P-Ch	-120			
		V_{DS} ≥ 4.5 V, V_{GS} = 8.0 V	N-Ch	400			
		V_{DS} ≤ -4.5 V, V_{GS} = -8.0 V	P-Ch	-400			
Drain Source On State Resistance*1	$r_{DS(on)}$	V_{GS} = 2.5 V, I_D = 150 mA	N-Ch		1.6	2.5	Ω
		V_{GS} = -2.5 V, I_D = -75 mA	P-Ch		4	5	
		V_{GS} = 4.5 V, I_D = 250 mA	N-Ch		1.2	2.0	
		V_{GS} = -4.5 V, I_D = -180 mA	P-Ch		2.6	3.8	
Forward Transconductance*1	g_{fs}	V_{DS} = 2.5 V, I_D = 50 mA	N-Ch		150		mS
		V_{DS} = -2.5 V, I_D = - 50 mA	P-Ch		200		
Diode Forward Voltage*1	V_{SD}	I_S = 50 mA, V_{GS} = 0 V	N-Ch		0.7	1.2	V
		I_S = -50 mA, V_{GS} = 0 V	P-Ch		-0.7	-1.2	
Total Gate Charge	Q_g	N-Channel	N-Ch		300	450	pC
		V_{DS} = 5 V, V_{GS} = 4.5 V, I_D = 100 mA	P-Ch		300	450	
Gate Source Charge	Q_{gs}	P-Channel	N-Ch		25		
		V_{DS} = -5 V, V_{GS} = -4.5 V, I_D = -mA *2	P-Ch		25		
Gate Drain Charge	Q_{gd}		N-Ch		100		
			P-Ch		100		
Input Capacitance	C_{iss}	N-Channel	N-Ch		15		pF
		V_{DS} = 5 V, V_{GS} = 0 V	P-Ch		15		
Output Capacitance	C_{oss}	P-Channel	N-Ch		11		
		V_{DS} = -5 V, V_{GS} =0 V *2	P-Ch		11		
Reverse Transfer Capacitance	C_{rss}		N-Ch		5		
			P-Ch		5		
Turn On Time	$t_{d(on)}$	N Channel	N-Ch		7	12	ns
		V_{DD} = 3 V, R_L = 100Ω	P-Ch		7	12	
Rise Time	t_r	I_D= 0.25 A, V_{GEN} = 4.5 V, R_g = 10 Ω	N-Ch		25	35	
			P-Ch		25	35	
Turn Off Delay Time	$t_{d(off)}$	P-Channel	N-Ch		19	30	
		V_{DD} = -3 V, R_L = 100Ω	P-Ch		19	30	
Fall Time	t_f	I_D= -0.25 A, V_{GEN} = -4.5 V, R_g = 10 Ω	N-Ch		9	15	
			P-Ch		9	15	

*1 Guaranteed by design, not subject to production testing.

*2 Pulse test; pulse width ≤300μs, duty cycle≤2%.